AM41V4, AM41V4ZC
4MPIX 500FPS CMOS IMAGE SENSOR

Description

AM41V4 is a 4 Megapixel High Speed 500 Frames/s CMOS Image sensor with Global Shutter and 4/3" optical format. It is a good solution for machine vision assembly lines, 3D scanners, special effects in movies, commercials, and for high speed TV broadcast.

AM41V4 CMOS Image Sensor is the 2nd generation High Speed CMOS digital image sensor product which follows the traditions of high speed architectures of Photobit Corporation (PB-MV40 and PB-MV13). The 2nd Gen shutter pixel is a buried channel device with reduced noise, and enhanced Blue sensitivity.

AM41V4 uses column parallel ADC converters to digitize the image. The sensor provides direct access to row addressing which allows the user to realize multiple Region of Interest (ROI) readout which is having multiple windows.

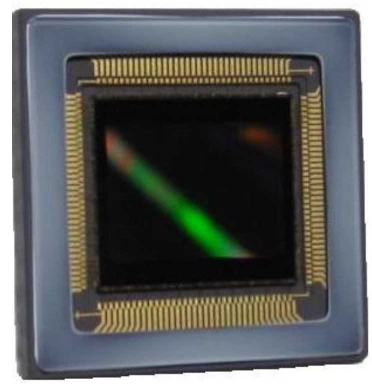

Fig.1. The photograph of a Color AM41V4 CMOS Image Sensor

Specifications

Optical format	4/3"
Resolution/ Active resolution	2368 x1728 / 2336 x 1728
Pixel	7um pitch 5T shutter pixel
Full well, AM41V4 / AM41V4ZC	20ke- in 5T; 45ke- in 3T mode / 15ke- in 5T
Noise, AM41V4/ AM41V4ZC	22e- / 18e-
Responsivity @550nm AM41V4/ AM41V4ZC	8V/Lux-s / 11V/Lux-s
QE	>40% @550nm
Conversion gain AM41V4/ AM41V4ZC	70 uV/e- / 95uV/e-
DSNU	0.5% r.m.s.
PRNU	1.5% rms
Row-wise noise*	0.3 DN rms
Dark current	25 mV/s @ 45C
Shutter efficiency	99.9%
Small-signal nonlinearity	<1% p-p
Nominal Frame Rate	500 Frames/s @full resolution
Maximum Frame Rate	700 Fps, degraded 7b ADC performance
Column ADC	SA ADC, 10b
Gain Options	X2, X4 and through ADC reference
Data Output	16 ports 10b CMOS 1.8V
Nominal Clock rate	133 MHz
Power supply	3.3V Analog, 1.8-2.1V digital
Power consumption	1.7 W @500Fps
Package	280 micro-PGA, 36mm/side
Color	PGB or Mono

*May be specific to particular characterization board design

REVISION HISTORY

Date	Revision	Comments
06.05.12	1.0	First revision made of AM41_ICD_7D

1.0 BLOCK DIAGRAM

The block diagram of the A40-AM41 sensor is drawn in Fig.1.

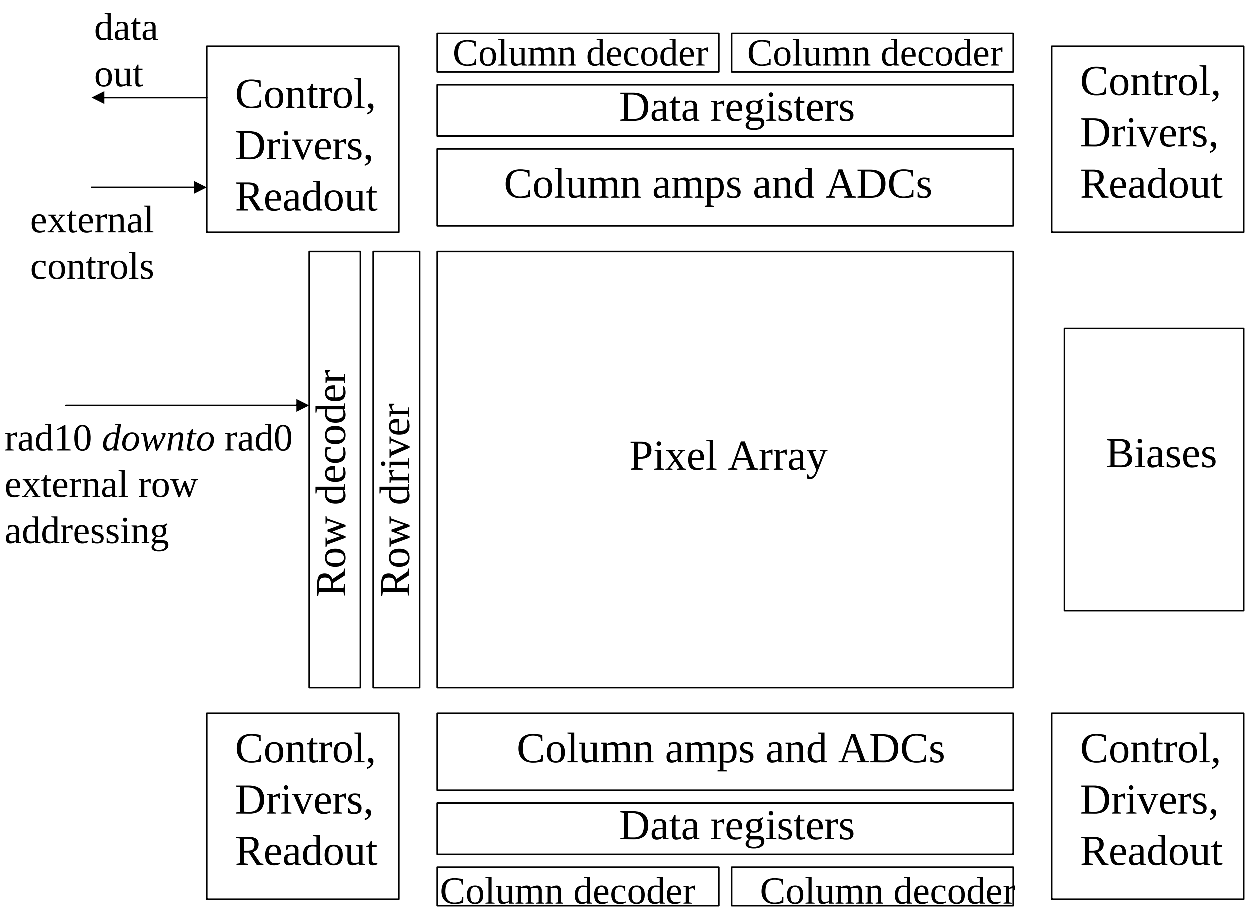

Fig.2. AM41 Sensor block diagram

The sensor has two column readout blocks (on top and in the bottom) which include per-column sample circuits, amplifier circuits, and ADCs with readable SAR (successive-approximation) registers, where the ADC data is temporarily stored for readout. The readout from the SAR registers as well as the sensor controls are arranged as a 4 quadrant readout & control architecture, which allows local control over SAR ADCs and local data readout, both essential for high speed operation of the sensor. The sensor also has some biases and all current sources generated internally. Although, many critical voltages to this chip are required to be generated externally.

2.0 PIXEL ARRAY

There are total of 2368x1728 pixels.

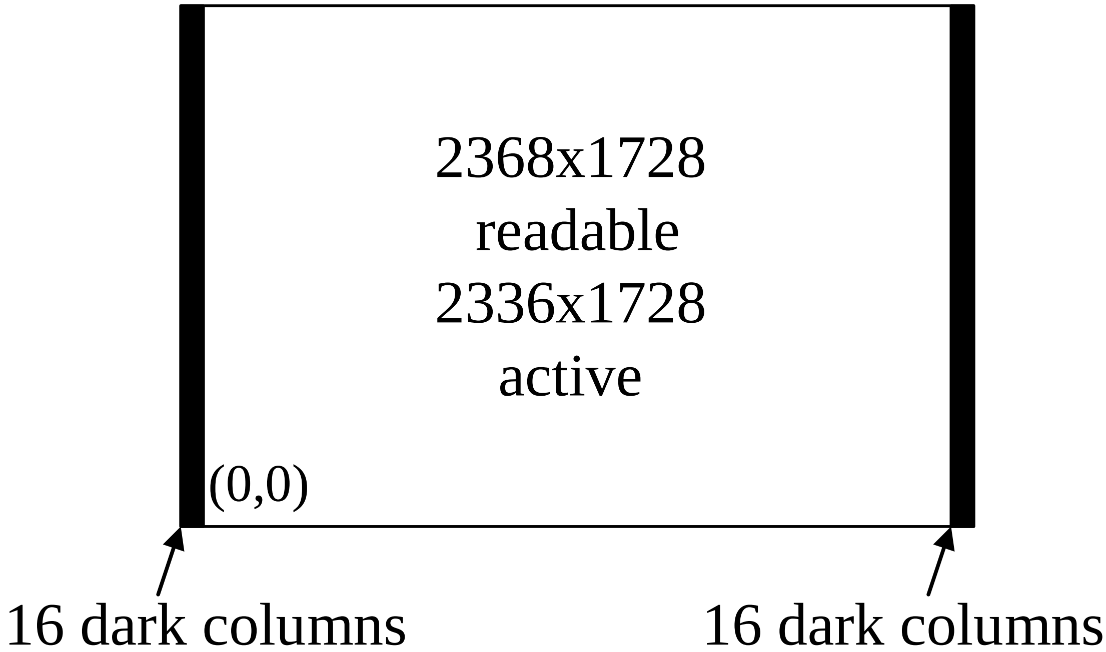

Fig.3. Definition of readable (black + active) and active pixel array. Column 0 is the first dark column.

Black pixels were added in the second revision of the sensor.

3.0 PIXEL GLOBAL SHUTTER CONTROLS

The 5T (five transistor) shutter pixel has the following controls: *PRST_n*, *TX_n, and PD_n* to help to setup the global exposure and operate the pixel. The controls work as follows:

- *'PD_n'* (applied to AB gate). When low, allows for exposure. When high, makes the reset of the photodetector PD
- *'TX_n'* (transfer pulse) *("low")* make the transfer of charge from the photodetector PD to the pixel memory FD
- *'PRST_n' ("low")* resets the pixel memory FD. Together with *'TX_n'* can reset both the memory and the photodiode.

So, if one needs to clear the entire pixel, such as in case of after a long pause, PD_n is made high, and TX_n and PRST_n are made LOW, and the pixel cleared of the accumulated dark current charge.

During the signal readout from the pixel the sensor control block generate an internal sequence of pulses. These operations include the readout of the signal stored at FD node, reset of the pixel using PRST and TX controls (local to the row selected for readout), and reading out the signal corresponding to the reset pixel.

AM41 pixel may operate in 3T mode with Full Well Capacity (FWC) enlarged to 45ke- by adding TX capacity to FD-node. To achieve this, one should keep TX_n LOW. There are 2 modifications of AM41 based on the value of FD capacitance: the standard 20ke- FWC/ 8V/Lux-s pixel and the enhanced sensitivity pixel 15ke- FWC / 11V/Lux-s.

4.0 TIMING IN CONTINUOUS MODE

Sensor controls assume an external row addressing (row0- row10) using a simple binary encoding. The addresses corresponding to the active pixels are the ones 0 through 1727. To read from the selected row of pixels and perform A-to-D over pixel signals, one needs to send a Start Row control "st_row_n". Reading out one pixel row and the digitization take certain number of clocks. This number is matched to the number of clocks needed to transfer all the digital data out of the chip. So, after the digitization of the pixel signals from the first row is completed, one may send the control Start Read ("st_read_n") to read the digital data out. Simultaneously, one may apply Start Row pulse to the next selected row. The readout rolls row after row, and these two controls present in all rows except for the first one (when Start Read is not needed; no ADC data yet) and the last one (when another Start Row is no longer needed, but Start Read still needs to be applied to read out the ADC data from the last row).

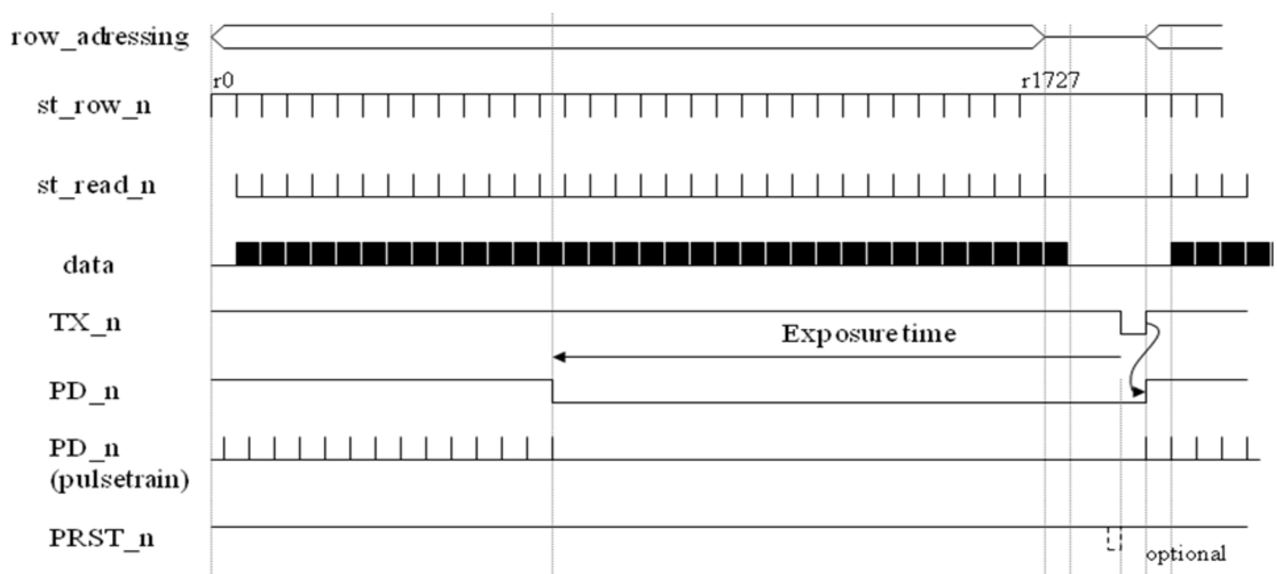

Fig.4. An example of one frame timing in continuous operation

An example of the frame timing with exemplary global shutter controls is drawn in Fig.4. We suggest two options for exposure control. In a simple implementation, PD_n is always high except for exposure time and during the transfer pulse. In a more advanced implementation, the photodiode is cleared with a pulsetrain of PD_n pulses, one pulse per row time. The charge transfer is accomplished with *TX_n* low. Optional PRST_n pulse in Fig.4 just before TX_n can be tried to additionally clear the pixel memories before the readout. *It was found experimentally, that the optional RST pulse may cause top-bottom shutter artifact in combination with a single step-wise PD_n. This was not checked for using PD_n pulsetrain yet.* The abovementioned pixel memories are also cleared during the readout process.

This timing diagram is designed for continuous sensor operation when the exposure overlaps with the readout, and the exposures is less than the frame time. If the exposure is equal to the frame time, one option is to omit the *PD_n* (high) pulse.

The length of TX_n is recommended to be 50-190 clocks. The exact position of the global PD pulse edge (as exposure start) inside row timing affects the appearance of the shutter line.
To remove a static shutter line, one has to end PD_n pulse at the position inside one row drawn in Fig.5., between clocks 90 and 150. By fixing the position of the edge inside the row, the exposure time would be quantized with the minimum time change equal to one row time.

In the sensor running continuously, an exposure change may cause a shutter line in the “change” frame. If the user is concerned about this artifact, we recommend to switch to a pulse-trained PD_n, where PD_n HIGH is enabled for ~8 clocks in every row where PD must be cleared. The approximate position of the single pulse in pulse-trained PD_n is shown in Fig.5.

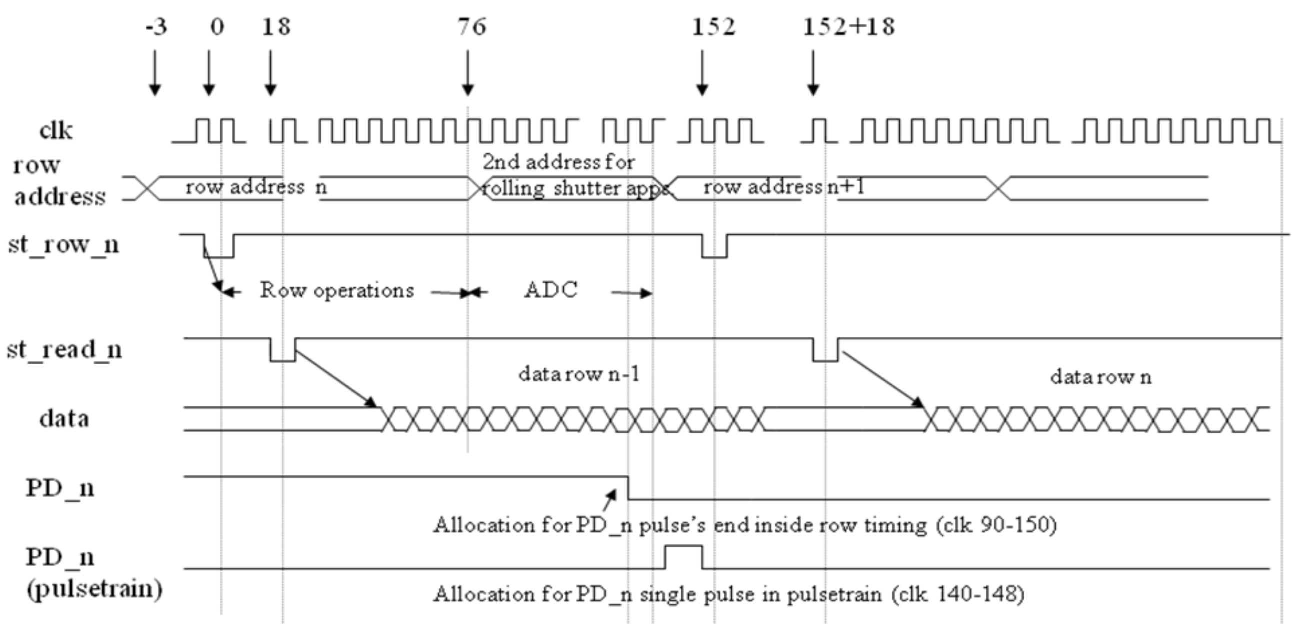

Fig.5. Example of one row timing

We recommend row time be 152 clocks (high speed operation mode) or 208-210 clocks (low frame rate “quiet” mode). In the quiet mode, the data from the sensor being output for 148 clocks do not overlap with sensitive pixel read operations, so there is less risk to catch up data noise.

We recommend to set up row address at least 2-3 clocks prior to sending Start_row_n command (a one-clock LOW pulse) and keep the row address at least for 76 clocks since the Start_row_n. During this time, signals from the pixels are read down into the column ADCs. Changing the row address a few ckock cycles before the Start_row_n eliminates static horizontal lines on the left and on the right.

The row address is kept for 152 clocks and then changed 2-3 clocks before Start_row_n for the next row. This timing is recommended for Global Shutter Operation. A limited number of users may want to operate the pixel in a Rolling Shutter mode. Then clocks 76 through 149 can be allocated to the Second Reset Pointer needed in the rolling shutter routine. The second reset then needs to be enabled in the timing through the register "Sndrst_enb"=0.

Reading out the digital data of one row from the sensor is initiated with Start_read_n command (one-clock* LOW pulse). We recommend to send Start_read_n at 18th clock after Start_row_n. There is a latency between Start_read_n and actual Data out of about 3-4 clocks (needs to be determined experimentally).

In high speed operation mode (row time=152 clocks), we recommend a 18 clock delay of the Start_read to Start_row. This reduces the ground noise pickup in half compared to the case Start_read and Start_row start together, and has no impact on the frame rate.

*) Start_row and Start_read extract the control from the falling edge of the control, so the duration of LOW is not really important, but it must be at least 1 clock.

If highest possible speed from the sensor is not needed, and row time can be extended to 210 clocks (quiet operation), then Start_read must go with 73-75 clk delay to Start_row (73 clk for 208 clock row). In this mode the pickup of the ground noise by the sensor is minimized.

Output data starts with 16 dark columns on the left from the ports 10-17, and with the active pixel data from the middle of image, from the ports 20-27. The direction of the data read (left –to middle) for ports 10-17, and from the middle to the right (ending with 16 dark columns) – from ports 20-27.

5.0 TIMING IN SEQUENTIAL (EXTERNAL TRIGGER) MODE

After reading Sections 3.0 and 4.0 a proficient user may generate his own timing diagrams for the case of the sequential global shutter operation. Under sequential shutter one typically understands the operation when the exposure does not overlap with the pixel readout. This type of readout can not maximize the sensor frame rate. This readout usually required when synchronizing the sensor operations with an external trigger. We recommend that PD_n control in "waiting" mode is always HIGH. On the trigger command, sensor shall start the exposure (PD_n goes LOW). The exposure is ended with sending the transfer pulse TX_n low. More exactly, with the rising edge of TX pulse. Just before the transfer pulse we need to clear FD memory nodes by sending global PRST_n low pulse.

6.0 OUTPUT PORTS

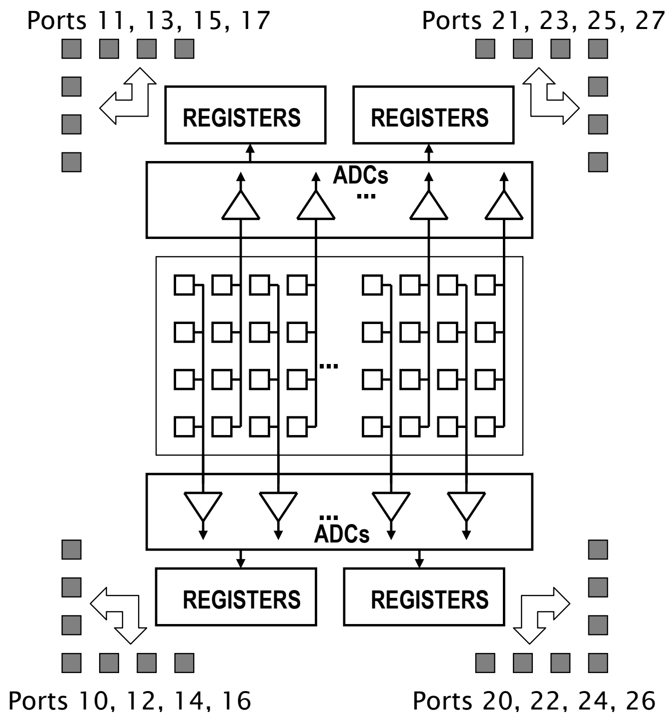

Fig.7. Output ports

AM41 has 16 ports 10 bit each. Although the ADCs are implemented as a uniform column-parallel block (one at the bottom of the sensor, one on the top), the data registers which store the ADC data are split into the left and the right ones, so that the left data registers serve only the left half of the pixel array columns, and the right – only the right ones. This was done to avoid having very long bit lines and associated delay.

The schematic drawing of the output port architecture is drawn in Fig.7.

7.0 SENSOR CONTROLS

7.1. Overview

There are four sensor control blocks in the four corners of the chip. The two upper control blocks serve the upper readout, the two bottom control blocks serve the bottom readout. The upper internal controls are somewhat autonomous from the bottom controls. Small timing misalignment between the top and the bottom internal control pulses shall not cause any conflict of drivers. But, there shall be good symmetry of operation between the left and the right controllers, because they are driving column ADCs from both sides. To facilitate this symmetry, the chip master clock is split into the *clk_top* and *clk_bot* serving the top and the bottom of the chip, respectively. Also, the clock pads are placed in the middle of the pad ring (at the top, and bottom) to built a clock tree which is left-right symmetrical.

Row driver is placed on both lift and right sides of the chip, the global shutter controls are registered so they normally arrive at the same time to the row driver. However, if setup time is very short, it may happen that the left and the right control will be sampled by different clocks which **may cause the appearance of random broken lines in the image**.

There are two important controls start_row_n and start_read_n which trigger row operations and readout operations. These pads are on the left side of the chip, so their propagation time to the left and the right controllers are different. The difference can reach ~ 4 ns. This dictates a long setup time for these two pulses to exclude the situation when the left controller senses the "Start" command one clock earlier than the right controller, which may cause a chip malfunction.

Serial interface commands and the clock experience long internal delays. These controls use weak drivers over long distances. The clock frequency is recommended to be at least 1/10 of the master clock frequency.

Master Clock. ***Clk_top*** *and* ***Clk_bot*** are 50-133 MHz for 350-500 Frames/s operation. Duration +-10%. **It is desirable that the clock to the bottom is synchronous to the top clock.** An equal length traces for top and bottom clock could be tried. However, there is a little mismatch in the package routing for these two pins.We recommend that the phase for the 3 clocks essential for the sensor operation which are the top and the bottom clocks and the data sampling clock, are fine adjusted separeately in the camera FPGA.

7.2. Setup and hold time for essential controls
Definition of setup/hold time is in Fig.4

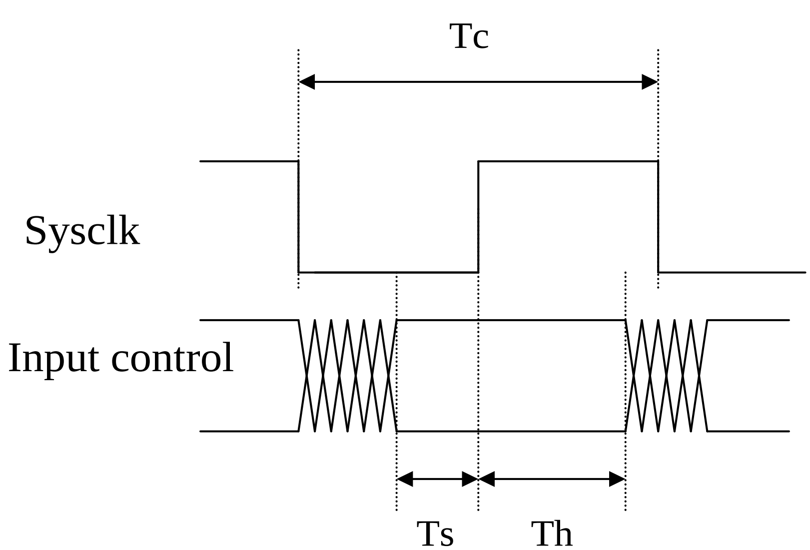

Fig.8.

For input controls st_row_n, st_read_n, use the following table

	Min	Typical	Max
Setup time Ts	5 ns		Tc- 0.5 ns
Hold time Th	0 ns	0.5 ns	

Since the recommended setup time is of the order of Tc/2, the standard choice of using the falling edge of the clock to start a control pulse may be problematic for these two controls. Rising edge plus some natural gate delay may work better.

The parameters of Lrst_n, Standby_n, are not critical.

The requirements to the timing of the serial interface are considered later.

Output data delay time with respect to the rising edge of clk_top, clk_bot.

	Min	Typical	Max
Data delay time Td*	1ns	2ns	4ns

*Load capacitance 10 pF and less

Both clock edges of the original clock might be tried to sample the data

OE: Asynchronous enable/disable of tri-state output pads

Rad0-Rad10. Asynchronous row select address. Setup time with respect to *st_row_n* control falling edge is 0. Row address may still change along with the negative edge of *st_row_n*.

8.0 DIGITAL I/O PADS ABSOLUTE RATINGS

AM63 and AM41 are **operated from 1.8V digital power supply.**

Anolog power supply voltage remains higher. We recomment 3V for VAA.

The pads have the following ratings:

	Operating condition	Min	Typ	Max
VDDIO	I/O Power, operating ratings	1.7V	1.8V	2.5V
VDDIO	I/O Power, absolute maximum ratings	-0.3V		2.5V
	Input digital I/O pads, logic LOW level	-0.3V	0V	+0.5V
	Input digital I/O pads, logic HIGH level	1.6V	1.8V	+2.5V
	Input digital I/O pads, absolute maximum ratings	-0.3V		+3.3V
	Output digital I/O pads, logic LOW level	-0.3V	0V	+0.5V
	Output digital I/O pads, logic HIGH level	1.6V	1.8V	+2.5V

9.0 PIN LIST FOR 1.27mm 280 uPGA

IO pin#	uPGA pin	AM63	AM41
1	D4	d15out2	d15out2
2	B2	d15out1	d15out1
3	C3	VDDIO	VDDIO
4	A1	GNDK	GNDK
5	C2	VDDK	VDDK
6	B1	d15out0	d15out0
7	D3	AGND	AGND
8	C1	VAA	VAA
9	E3	VADL	VADL
10	D1	VADH	VADH
11	F3	AGND	AGND
12	E1	VAA	VAA
13	G3	VRSTH	VRSTH
14	F1	d17out9	d17out9
15	D2	d17out8	d17out8
16	G1	d17out7	d17out7
17	H3	d17out6	d17out6
18	H1	VSSIO	VSSIO
19	E2	d17out5	d17out5
20	J1	d17out4	d17out4
21	J3	d17out3	d17out3
22	K2	d17out2	d17out2
23	H2	VDDIO	VDDIO
24	K1	d17out1	d17out1
25	K3	d17out0	d17out0
26	L2	TX_n	TX_n
27	J2	rad10	rad10
28	L1	rad8	rad8
29	L3	rad6	rad6
30	M2	rad4	rad4
31	G2	rad2	rad2
32	M1	rad0	rad0
33	M3	st_read_n	st_read_n
34	N2	VSSIO	VSSIO
35	F2	VDDIO	VDDIO
36	N1	GNDK	GNDK
37	N3	VDDK	VDDK
38	P2	st_row_n	st_row_n
39	P3	rad1	rad1
40	P1	rad3	rad3
41	R3	rad5	rad5
42	R2	rad7	rad7
43	X2	rad9	rad9
44	R1	rad11	PD_n
45	T3	PRST_n	PRST_n

46	T2	d16out0	d16out0
47	W2	d16out1	d16out1
48	T1	VDDIO	VDDIO
49	U3	d16out2	d16out2
50	U2	d16out3	d16out3
51	Y2	d16out4	d16out4
52	U1	d16out5	d16out5
53	V3	VSSIO	VSSIO
54	V2	d16out6	d16out6
55	AA2	d16out7	d16out7
56	V1	d16out8	d16out8
57	W3	d16out9	d16out9
58	W1	VTXHI	VABL
59	X3	VAA	VAA
60	X1	AGND	AGND
61	Y3	VADH	VADH
62	Y1	VADL	VADL
63	AA3	VAA	VAA
64	AA1	AGND	AGND
65	AB2	d14out0	d14out0
66	AB1	VDDK	VDDK
67	AB3	GNDK	GNDK
68	AC1	VDDIO	VDDIO
69	AC2	d14out1	d14out1
70	AD1	d14out2	d14out2
71	AB4	d14out3	d14out3
72	AD2	VDDK	VDDK
73	AC3	GNDK	GNDK
74	AE1	d14out4	d14out4
75	AD3	VSSIO	VSSIO
76	AE2	d14out5	d14out5
77	AC4	d14out6	d14out6
78	AE3	d14out7	d14out7
79	AC5	d14out8	d14out8
80	AE4	d14out9	d14out9
81	AC6	VDDIO	VDDIO
82	AE5	d12out0	d12out0
83	AC7	d12out1	d12out1
84	AE6	d12out2	d12out2
85	AD4	d12out3	d12out3
86	AE7	d12out4	d12out4
87	AC8	VSSIO	VSSIO
88	AE8	d12out5	d12out5
89	AD5	d12out6	d12out6
90	AE9	d12out7	d12out7
91	AC9	d12out8	d12out8
92	AD10	d12out9	d12out9

93	AD8	VDDIO	VDDIO
94	AE10	d10out0	d10out0
95	AC10	d10out1	d10out1
96	AD11	d10out2	d10out2
97	AD9	d10out3	d10out3
98	AE11	d10out4	d10out4
99	AC11	VSSIO	VSSIO
100	AD12	d10out5	d10out5
101	AD7	d10out6	d10out6
102	AE12	d10out7	d10out7
103	AC12	d10out8	d10out8
104	AD13	d10out9	d10out9
105	AD6	VDDIO	VDDIO
106	AE13	clk_bot	clk_bot
107	AC13	d20out9	d20out9
108	AD14	d20out8	d20out8
109	AC14	d20out7	d20out7
110	AE14	d20out6	d20out6
111	AC15	d20out5	d20out5
112	AD15	VSSIO	VSSIO
113	AD20	d20out4	d20out4
114	AE15	d20out3	d20out3
115	AC16	d20out2	d20out2
116	AD16	d20out1	d20out1
117	AD19	d20out0	d20out0
118	AE16	VDDIO	VDDIO
119	AC17	d22out9	d22out9
120	AD17	d22out8	d22out8
121	AD21	d22out7	d22out7
122	AE17	d22out6	d22out6
123	AC18	d22out5	d22out5
124	AD18	VSSIO	VSSIO
125	AD22	d22out4	d22out4
126	AE18	d22out3	d22out3
127	AC19	d22out2	d22out2
128	AE19	d22out1	d22out1
129	AC20	d22out0	d22out0
130	AE20	VDDIO	VDDIO
131	AC21	d24out9	d24out9
132	AE21	d24out8	d24out8
133	AC22	d24out7	d24out7
134	AE22	d24out6	d24out6
135	AD23	d24out5	d24out5
136	AE23	VSSIO	VSSIO
137	AC23	d24out4	d24out4
138	AE24	GNDK	GNDK
139	AD24	VDDK	VDDK

140	AE25	d24out3	d24out3
141	AB23	d24out2	d24out2
142	AD25	d24out1	d24out1
143	AC24	VDDIO	VDDIO
144	AE26	GNDK	GNDK
145	AC25	VDDK	VDDK
146	AD26	d24out0	d24out0
147	AB24	AGND	AGND
148	AC26	VAA	VAA
149	AA24	VADL	VADL
150	AB26	VADH	VADH
151	Y24	AGND	AGND
152	AA26	VAA	VAA
153	X24	VDD_PIX	VPIX
154	Y26	d26out9	d26out9
155	AB25	d26out8	d26out8
156	X26	d26out7	d26out7
157	W24	d26out6	d26out6
158	W26	VSSIO	VSSIO
159	AA25	d26out5	d26out5
160	V26	d26out4	d26out4
161	V24	d26out3	d26out3
162	U25	d26out2	d26out2
163	W25	VDDIO	VDDIO
164	U26	d26out1	d26out1
165	U24	d26out0	d26out0
166	T25	lrst_n	lrst_n
167	V25	Sdata	sdata
168	T26	Sclk	sclk
169	T24	Tr_en	Tr_en
170	R25	VLNT	VLNT
171	X25	VMUX1	VMUX1
172	R26	VMUX2	VMUX2
173	R24	VOFF	VOFF
174	P25	VLNA (VLP)	VLNA (VLP)
175	Y25	VTXL	VTXL
176	P26	AGND	AGND
177	P24	VAA	VAA
178	N25	VAD2	VAD2
179	N24	VREF	VREF
180	N26	VLN	VLN
181	M24	VRSTL_TST	VRSTL_TST
182	M25	VCAS	VCAS
183	G25	SH_4T	SH_4T
184	M26	OE	OE
185	L24	standby_n	standby_n
186	L25	d27out0	d27out0

187	H25	d27out1	d27out1
188	L26	VDDIO	VDDIO
189	K24	d27out2	d27out2
190	K25	d27out3	d27out3
191	F25	d27out4	d27out4
192	K26	d27out5	d27out5
193	J24	VSSIO	VSSIO
194	J25	d27out6	d27out6
195	E25	d27out7	d27out7
196	J26	d27out8	d27out8
197	H24	d27out9	d27out9
198	H26	VDD_PIX	VPIX
199	G24	VAA	VAA
200	G26	AGND	AGND
201	F24	VADH	VADH
202	F26	VADL	VADL
203	E24	VAA	VAA
204	E26	AGND	AGND
205	D25	d25out0	d25out0
206	D26	VDDK	VDDK
207	D24	GNDK	GNDK
208	C26	VDDIO	VDDIO
209	C25	d25out1	d25out1
210	B26	d25out2	d25out2
211	D23	d25out3	d25out3
212	B25	VDDK	VDDK
213	C24	GNDK	GNDK
214	A26	d25out4	d25out4
215	B24	VSSIO	VSSIO
216	A25	d25out5	d25out5
217	C23	d25out6	d25out6
218	A24	d25out7	d25out7
219	C22	d25out8	d25out8
220	A23	d25out9	d25out9
221	C21	VDDIO	VDDIO
222	A22	d23out0	d23out0
223	C20	d23out1	d23out1
224	A21	d23out2	d23out2
225	B23	d23out3	d23out3
226	A20	d23out4	d23out4
227	C19	VSSIO	VSSIO
228	A19	d23out5	d23out5
229	B22	d23out6	d23out6
230	A18	d23out7	d23out7
231	C18	d23out8	d23out8
232	B17	d23out9	d23out9
233	B19	VDDIO	VDDIO

234	A17	d21out0	d21out0
235	C17	d21out1	d21out1
236	B16	d21out2	d21out2
237	B18	d21out3	d21out3
238	A16	d21out4	d21out4
239	C16	VSSIO	VSSIO
240	B15	d21out5	d21out5
241	B20	d21out6	d21out6
242	A15	d21out7	d21out7
243	C15	d21out8	d21out8
244	B14	d21out9	d21out9
245	B21	clk_top	clk_top
246	A14	VDDIO	VDDIO
247	C14	d11out9	d11out9
248	B13	d11out8	d11out8
249	C13	d11out7	d11out7
250	A13	d11out6	d11out6
251	C12	d11out5	d11out5
252	B12	VSSIO	VSSIO
253	B7	d11out4	d11out4
254	A12	d11out3	d11out3
255	C11	d11out2	d11out2
256	B11	d11out1	d11out1
257	B8	d11out0	d11out0
258	A11	VDDIO	VDDIO
259	C10	d13out9	d13out9
260	B10	d13out8	d13out8
261	B6	d13out7	d13out7
262	A10	d13out6	d13out6
263	C9	d13out5	d13out5
264	B9	VSSIO	VSSIO
265	B5	d13out4	d13out4
266	A9	d13out3	d13out3
267	C8	d13out2	d13out2
268	A8	d13out1	d13out1
269	C7	d13out0	d13out0
270	A7	VDDIO	VDDIO
271	C6	d15out9	d15out9
272	A6	d15out8	d15out8
273	C5	d15out7	d15out7
274	A5	d15out6	d15out6
275	B4	d15out5	d15out5
276	A4	VSSIO	VSSIO
277	C4	d15out4	d15out4
278	A3	GNDK	GNDK
279	B3	VDDK	VDDK
280	A2	d15out3	d15out3

11. PIN DESCRIPTION

Data out *(16 x 10 pins)*- digital output. Format: *d*-n-*out*-m e.g. *d5o4*, where n is the number of the port, m denotes the bit significance: m=9 is MSB, m=0 is LSB. Ports 10-17 output the first 0-1183 columns including the left 16 dark columns of the pixel area in the groups by 8 columns per clock. Ports 20-27 output the columns 1184 through 2367 in the groups by 8 columns per clock. The readout direction is left –to-right. It takes 148 clocks to read all columns. Output data I/O pads are tri-stated 16mA current pads. Output is enabled by applying HIGH to the *OE* pad

Lrst_n - sensor logic reset. LOW resets all flip-flops on the sensor. Recommended is reset on at least power-up (1-2 clocks asynchronous reset).

Standby_n- LOW bring sensor in low power mode.

SH_4T – must be HIGH in Rev.2 and up of the sensor. (As of 2011 we supply revisionsV3 (very limited) and V4)

Rad0-Rad11- sensor row address (binary)

St_row_n – Edge High-to-Low initiates pixel read operations in selected row followed by ADC.

St_read_n – Detected by High-to-Low transition. Dumps data from the ADC registers to data readout registers (1 clock) and launches column decoder for reading out column data registers.

VDDIO and ***VSSIO*** – digital I/O power and ground, **1.8V**. Instantaneous current driving 160 of 10pF loads may reach +-3A. The current averaged over data period is, theoretically, +-300 mA. The effective average pulse current is less because the data is stochastic, and in case of the Gray-coded data.
Operating sensor at higher frame rates (e.g. 500-600 fps) may require higher VDDIO, up to 2.2-2.3V. However, higher VDDIO may cause more row-wise noise.

VDDK and ***GNDK*** – core digital power and ground, Default VDDK is **1.8V**. Higher clock operation may require raising VDDK to 2.1-2.3V.Consumption is ~1/10 of VDDIO.

VAA and ***AGND*** are analog power and ground. Recommended *VAA* value is 3.3V.
To reduce the overall power, user may also try VAA or 3.0V and below.
Expected dc current consumption from VAA source is 100 mA. There will also be a noticeable ac component of ~20-40 mA. It needs good decoupling.

VPIX. (was named *VRST_PIX* in Rev1-Rev4 of ICD) is to be finalized during the sensor characterization. Overall range is 2.0V to 3.3V . **We initially RECOMMEND 2.6V**. This voltage resets 2368 columns of pixels. Disabled 2-3 times during one row time, depending on the sensor mode. So, the consumption jumps from 0 mA to ~30 mA, staying at this consumption most of time. However, every time power is restored, it also charges a 2-4 nF parasitic all column capacitor. This is hundreds of mA of peak current. The worst scenario is when row addressing is stopped (such as an external trigger mode) then restarted. Then, suddently, the consumption grows from 0 to the level above. A large decoupling capacitor won't stabilyze the voltage. So, a separate regulator would probably be the best solution for cameras with modes extending over the regular continuous operation.

VADH- ADC High reference voltage, 0.2- 1.0V, nominal =0.9V. Requirements are equivalent to Vref1 voltage in MV-family of high speed sensors. Equivalent circuit: charges a 4 nF capacitor once in a row time. Shall settle within 1 mV for ~20 ns or have pulsations less than 1mV. If row operations stopped (No Start_row_n signals), there is no consumption from this pin. We recommend 1uF ceramic capacitor on each pin and one 500uF additional capacitor.

VADL- ADC low reference voltage, can be connected to *AGND* at the point *VADH* has a filter to *AGND.*

VAD2 –second ADC reference voltage, Shall be ½ of VADH. The requirements are 250X weaker than those to VADH

VRSTL_TST- this is a double functionality voltage. It serves as a test voltage for ADC and column circuit tests. Shall graduate change from 0 to 1.2V in this mode. Sensor users are not supposed to run these tests. Main function is the row driver anti-blooming voltage. Fixed at ~0.6V based on the sensor characterization. Charges a 4pF capacitor few times a row time. The worst loading condition is during global shutter reset. Charges ~2-4 nF capacitor for ~100 ns. In terms of coupling to the signal is less critical compared to *VTXH* and *VRSTH* (below)

VRSTH- row driver voltage 2.5-3.5V. **Initially, we recommend 3.4V**. Same loading conditions as for *VLO_VTEST*. But, the noise from this supply is injected directly to the signal.

VABL- row driver voltage 0-0.7V. Same requirements as to *VLO_VTEST*. **Initially, we recommend 0.2V.**

VTXL- pixel transfer gate low voltage -0.4 +0.0V. **Initially, we recommend 0V.**

For the best anti-blooming performance, when operating with the fully open shutter and trying to avoid the negative effect of very bright reflections on the data shuttered in the pixels in the previous frame, we recommend ***VABL*** *to be +0.2V, and* ***VTXL*** *to be -0.3V (negative!).*

VREF- column amplifier reference voltage 1-2V. This bias does not consume DC current. However, it is very critical from the point of view of readout noises. We recommend **1.35-1.4V**. A proper decoupling is needed for this pin.

VOFF- an offset voltage added to all columns. The sign is controlled digitally via Bit1 of serial interface. Requirements: 1/20 of those for *VADH*. Added to ADC signal with 1/20 attennuation. Voltage range 0- 1.2V with default value of ~0.7V. Higher Voff may cause ADC DNL which can be avoided with higher VDDK. **A proper decoupling is needed for this pin.**

VCAS – amp N cascode voltage, VREF+0.15V, low power bias. Initially, we recommend **1.55V**.

VLN, VLNT – current biases generated internally, may need override**. Initially, we recommend to keep these floating. If the biases are connected to a DAC in the design, we recommend 0.45V for VLN and 0.9V for VLNT.**

Higher VLN (0.5-0.6V) improves small signal linearity of the signal chain to <1%, reduces built-in positive offset and increases pixel saturation charge at the expense of a smaller gain from the pixel and slightly higher column FPN.

VLNA- column amp current generated internally, may need override. **We recommend 0.95V for higher signal range and 0.85V for low power operation. There is a noticeable increase in current between 0.8 and 1V!** When operating in low power mode, VADH needs to be reduced to 0.8V.

VMUX1- multiplexed pad for external override to the following internal biases:
VCASNA, VCASVLN, VCASN2, VCASN3, all 0.8-1.5V
We recommend selecting (1,0) setting for VMUX1(see below) and applying 1.3V to the pin.

VMUX2- multiplexed pad for external override of one of the following:
VLN3, VLNT all 0.8- 2V
We recommend selecting (1,0) setting for MUX2 and applying 0.95V to the pin.

In a simplified camera design, VMUX1 and VMUX2 may be left floating w/o visible worsening in image uniformity.

12.0. SERIAL INTERFACE DESCRIPTION

Serial interface in AM41-AM63 serves one function: to write the 16 sensor settings into the sensor controllers. The sensor settings are written in using the following pins: sdata, sclk, Tr_en. Serial interface allows to enable/disable 16 sensor setting controls:

Bit0 Col_test_en
Bit1 Offset_sign
Bit2 Gain_X2_en
Bit3 Gain_bit1_en
Bit4 Gain_bit2_en
Bit5 Unipolar_ADC_mode
Bit6 Long_comp_decision
Bit7 Row_change_en_b
Bit8 Sndrst_en_b
Bit9 VLN_cas_en
Bit10-11 VMUX1: VCASNA, VCASVLN, VCASN2, VCASN3
Bit12-13 VMUX2: VLN3, VLN2
Bit14 TXextend/ADC_tst_en (together with Bit0)
Bit15 Gray_enable

Chip logic reset Lrst_n=0 sets all bits to default value of "0". **Recommended settings: Bit6, Bit9, Bit11, and Bit13 ="1" others 0.**

12.1. Description of the bits

Bit0, Col_test_en: '1' disables pixel readout and enables column test, where pixel signals are substituted with a pair of voltages: VTEST and AGND

Bit1, Offset_sign: The '0' makes the offset negative. '1' keeps it positive. Offset is always enabled in this chip, the value is controlled with VOFF voltage (which translates to ADC input with 20-30 times attenuation)

Bits2, 3, and 4 Programmable gain 1 to 8.

```
Gain= (1+Bit2)/(1/4+1/4*(Not Bit3) +1/2*(Not Bit4))
```

As offset is amplified with gain but corrected after gain with Voff, using sensor gain option requires Voff adjustment every time one changes gain. For the best result, operate with higher VLN of ~0.55V which makes the built-in positive pre-gain offset smaller. Compare with the gain option available through VADH adjust.

Bit5, Unipolar_ADC_mode: This bit switches the chip between two operation modes. The modes relate to unipolar/differential way of processing signals in the column circuits. They may differ by amount of row/column noise.

Bit6, Enables longer decision time for ADC comparator. Shortens the time for voltage settling.
It seems, 1 at this register helps to improve ADC performance
Bit7, Row_change_en_b: This control relates to optimization of the pixel FPN. There is a high possibility this control stays at default '0'.

Bit8, Sndrst_en_b: Also, relates to pixel FPN and shutter operation. Will be optimized during the sensor test.

Bit9, VLN_cas_en: This control enables cascoding in the VLN buffer and may reduce one of the column fpn components. By default, it enables the circuit w/o cascoding.
Bit10-11, VMUX1: Connect one of the following internal biases VCASNA (00), VCASVLN (01) , VCASN2 (10), VCASN3 (11) to the common I/O pad VMUX1 for debugging/override purposes. (01) means bit10='1', bit11='0'.

Bit12-13: This controls connect one of the internal biases VLN3 (00) and VLNT (01) to the pad VMUX2.

Bit14, ADC_tst_en: When '1' this control disconnects the ADC from the output of the column amplifier, and substitutes the amp signal with a pair of voltages VTEST and AGND.

Bit15, Gray_enable: High enables Gray encoding for the output data after sensamps. This is expected to reduce the amount of row-wise noise at major transitions.

12.2. Timing of the interface

The serial interface is a D-flop shift register clocked by Sclk. Every rising edge of Sclk samples new Sdata into the register and moves the data written before by 1 bit. 16 Sclks update the entire register. **The bit written first is the bit #15 (the last bit).** For new register data to take effect on the image sensor, one needs to apply a Transfer enable (Tr_en) HIGH pulse, and on the first Low-to-Hign transition of the Clk_top (Clk_bot), the new register data is overwritten into the Digital Block registers.

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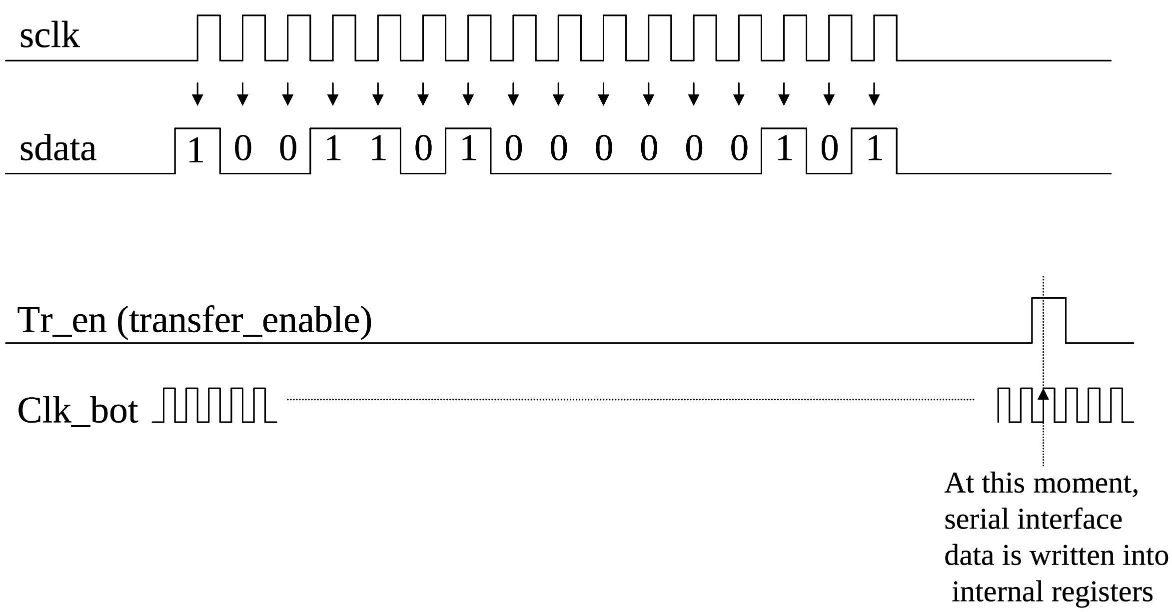

Fig.9. Operation of the serial register in the sensor setting mode.

13.0. MULTI-SLOPE HIGH DYNAMIC RANGE MODE

The pixel allows shuttered high dynamic range mode by implementing set of exposures and enabling a deeper capacity of FD in a step-wise fashion. The first exposure overlaps with the readout, and is controlled with PD_n position. The second and the third exposures are done in

Vertical Blank time. The vertical Blank time is the time between the frame readouts. VB includes the global shutter Transfer time. During VB, VRSTH is changed in step-wise fashion from high to low voltage.
User needs a powerful DAC or a DAC with a fast powerful driver to drive the VRSTH on-chip capacitance of ~ 5nF.

The detailed description of the implementation of the HiDy mode will be given in Addendum to Rev.6 of the ICD.

14.0. HIGH PIXEL CAPACITY MODE

Some inspection applications require high pixel capacity. AM41 allows Doubling of the full well capacity at the cost of losing the true global shutter operation.

In the high pixel capacity mode, the capacitance of the transfer gate is added to the capacitance of the readout node, and so the pixel becomes the rolling shutter 3T pixel with photodiode as a current source.

The simultaneous image acquisition then can be restored with operating with LED pulse shot in the Vertical Blank interval.

To switch the sensor into 3T mode with enlarged pixel capacity, the controls are modified as follows:
TX_n : Always 0.
PD_n: Always 0.

Recommended biases:
VLN=0.45V, VPIX=2.6V, VRSTH=3.45V.

15.0. APPLICATION NOTES ON GROUND NOISE; EXEMPLARY CIRCUITS

CMOS sensors, unless implemented on exotic SOI substrates or thinned BSI substrates have low-resistance connection between all sensor grounds such as Digital I/O ground, Digital Core ground, Analog Circuit and Pixel Array ground through sharing the same low-resistance substrate. We measured the typical resistance between any Digital Ground and adjacent Analog Ground be 3 Ohm. This is almost a short-circuit.

Single Ground Plane.

Because of the short between the analog ground and the digital ground on the sensor, it does not usually make sense to have separate Digital and Analog ground on the Sensor board in a camera. An example of sensor biasing and grounding using Single Ground plane is shown below.

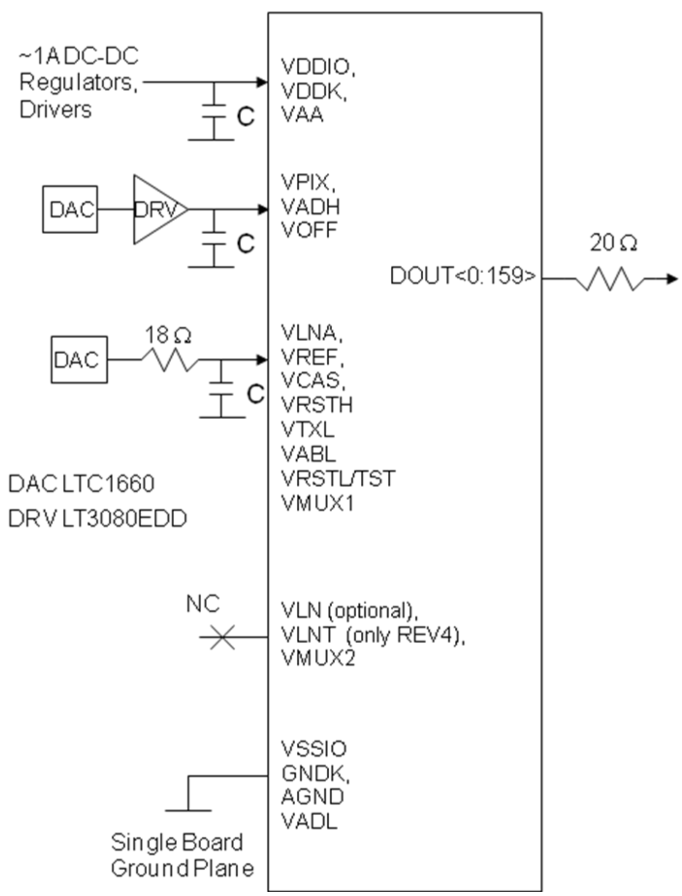

Fig.10. Example of connecting the sensor to the board with the Single Ground plane.

If a compact camera implementation is desired, VOFF may be generated with DAC, VTXL, VRSTL and VABL are grounded, and VMUX1 is added to NC (non-connect) list. Then, VRSTH may be combined with VAA and made 3.3V.

Recommended decoupling capacitors:

Voltage	Decoupling capacitor
VDDIO	0.1uF ceramic on each pin + 1uF ceramic +47uF electrolytic
VDDK	0.1uF ceramic on each pin + 1uF ceramic +470uF electrolytic
VAA	0.1uF ceramic on each pin + 4 (in each corner) 1uF + 220uF electrolytic
VADH	1uF ceramic directly(!) on each package pin +10uF+ 470uF electrolytic
VOFF	1uF ceramic +47uF electrolytic
VRSTH	1uF ceramic +47uF electrolytic
VPIX	2X 1uF ceramic + 220uF electrolytic
VLN	a) leave no-connect otherwise b) 1uF ceramic +22uF electrolytic
VREF	1uF ceramic +22uF electrolytic
VCAS	0.1nF ceramic
VLNT	a) leave no-connect otherwise b) 0.1uF ceramic
VMUX1, VMUX2	a) leave no-connect otherwise b) 0.1uF ceramic
VLNA	1uF ceramic +22uF electrolytic
VRSTL, VABL, VTXL	1uF ceramic +22uF electrolytic

Ground Noise in AM41 connected to Single Ground plane.

The dominant source of the ground noise in AM41 is the data-dependent AC current in powerful CMOS drivers (there are total of 160 output I/O data drivers each may be driving the peak current up to of 20 mA, data dependent!) and in the load. The transient driver current and the return current flow through the ground connection between the sensor and the board ground plane. Unfortunately, the package inductance and the wire-bond inductance are noticeable, of the order of 5 nH/ pin. When high frequency current flows through inductance, an e.m.f. is generated between the board ground plane and the sensor internal ground. The sensor ground is no longer the Clean Board ground. However, the critical sensitive biases coming to the sensor externally, are still decoupled to the Clean ground. However, the sensor sees these biases as noisy ones with respect to its substrate which is pulsing. This is demonstrated in the equivalent circuit in Fig.11. below.

Ground noise shows as a common-mode noise for all pixels being read simultaneously. We measure 0.5 DN rms of row-wise noise from the sensor with floating VLN, and up to 1 DN rms of the noise in the sensor with decoupled VLN. Ground noise in Am41 with Single Ground plane connection could be reduced by a) adding current limiting termination resistors to Data Output lines b) Reducing VDDIO voltage (slows down data out), c) reducing capacitive load to the sensor outputs, d) using floating VLN, and e) using Black Columns to subtract the common-mode noise.

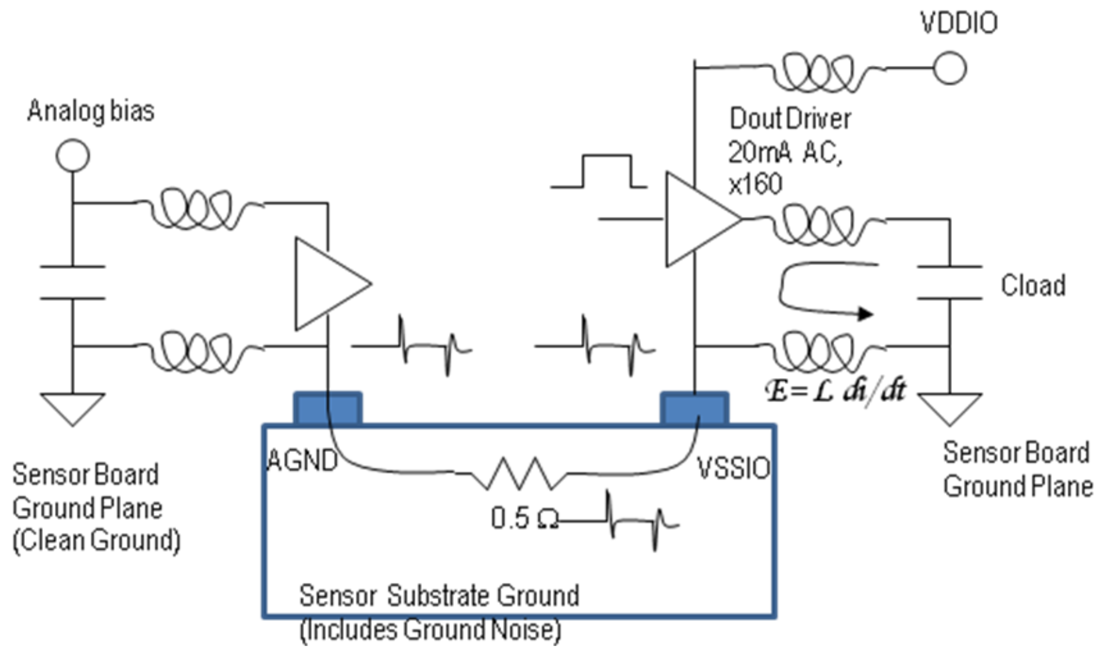

Fig.11. Ground noise in circuit with Single Ground plane. Analog bias to the sensor filtered to the clean board ground is seen by the sensor as noisy, because the sensor substrate includes data-dependent ground noise.

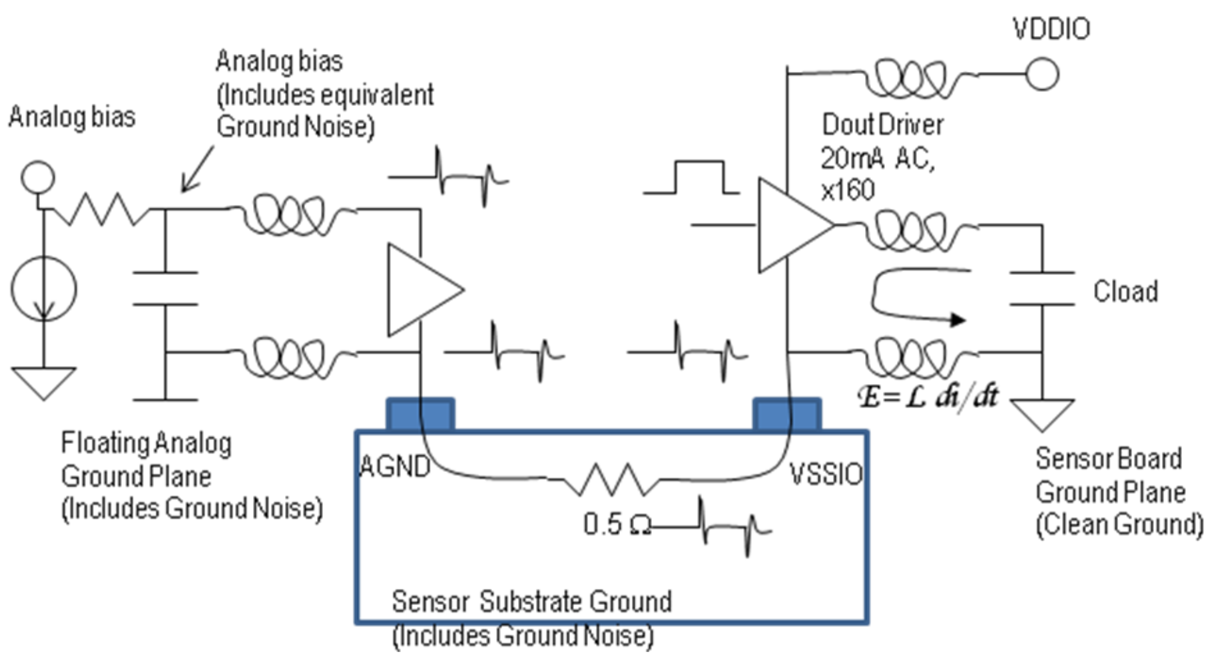

Fig.12. Ground noise in circuit with Floating Analog Ground plane. Analog bias to the sensor is filtered to the noisy ground coming from the sensor so the bias is Clean as seen by the sensor.

One question what if both Analog and Digital power supply originally come from the same regulator, which ground is connected to the single board ground (Fig.12). Then, if the bias is generated by a DAC or a driver, the DAC's ground is connected to the Floating Analog ground, while the power – to the filtered regulator voltage. In this case, the return current into regulator will flow through the sensor connection between the analog and the digital ground, which is not a problem.

Floating Analog Ground plane.
Because the sensor ground is noisy, there is an idea to take this noisy ground and decouple all sensitive biases to the sensor, to this noise ground.

In one implementation, ½ of all analog grounds are disconnected from the Single Ground Plane and connected to create a Floating Analog Plane. All analog biases to the sensor have decoupling capacitors to this Analog Ground plane. (See Fig.13).

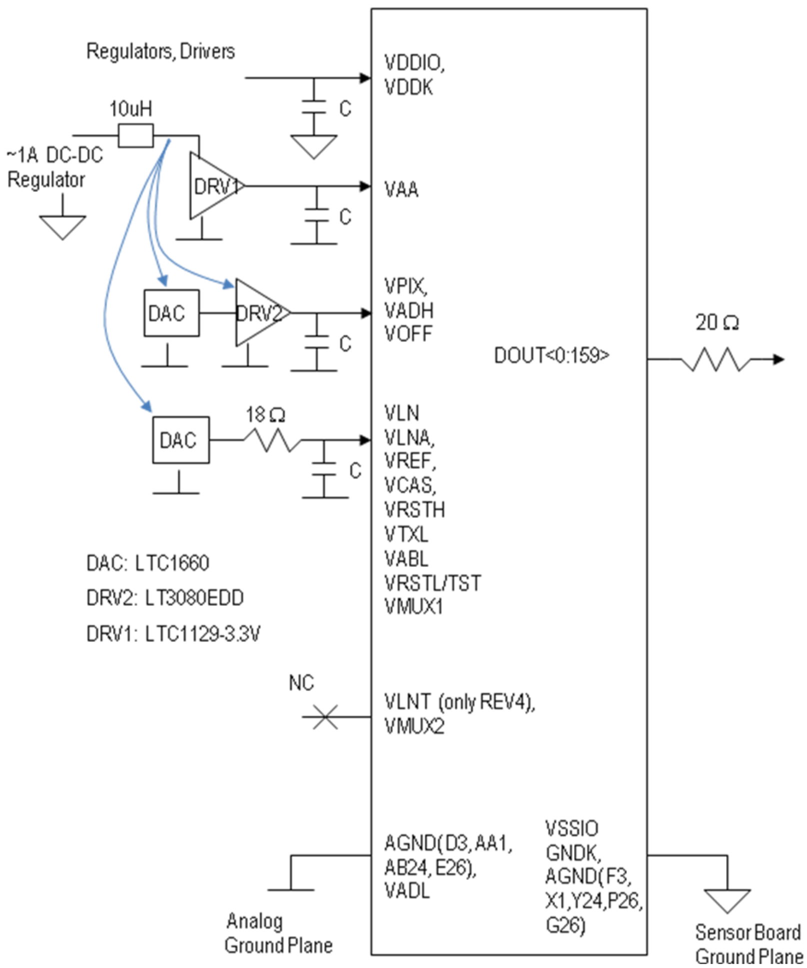

Fig.13. Example of connecting the sensor to the board with filtering of the biases to the Analog Ground plane created with ½ of the AGND pins from the sensor.

16.0 POWER-UP SEQUENCE

Typically, the sensor is not sensitive to power start up sequence. However we had one case of particular board and firmware, when certain percentage of sensors did not start properly. They showed excessive ADC DNL. If you experience the sensor gets stuck into low ADC resolution mode and lrst_n does not help, you may need to do an experimenting with power up sequence. In that particular case, applying VDDK prior to the clock and to other power voltages helped to get a correct sensor initialization.

17.0 WINDOWING, REGIONS OF INTEREST (ROI)

The sensor with column-parallel A-D converters typically has the row time fixed to whatever time is needed to read out from the pixels and perform A-D conversion. In AM41, this time is 150 clock cycles minimum, 158 clock cycles recommended, and is over 210-222 clock cycles in the super quiet mode (When Start_read is sent after 74^{th} clock since Start_row so the noisy data read does not overlap with sensitive pixel read operations).

As the row time is fixed, the windowing in the X direction can not increase the frame rate, so the capability to skip unwanted column data is not implemented in the sensor. For users who do not need all data in the row, we recommend *skip sampling the unwanted data* from the sensor output.

Opposite to X-windowing, AM41 sensor is very favorable for implementing windows in Y direction. The sensor does not include any Frame timing engine. Its operation is purely based on the processing of One line of the image which can be selected arbitrarily using Open Row Addressing Interface. All 11 bits of the row addressing are available to the user for control. So, the image can be constructed from the single lines read out in the random order. Similarly, several groups of the windows (Fig. 14) can be selected and read out.

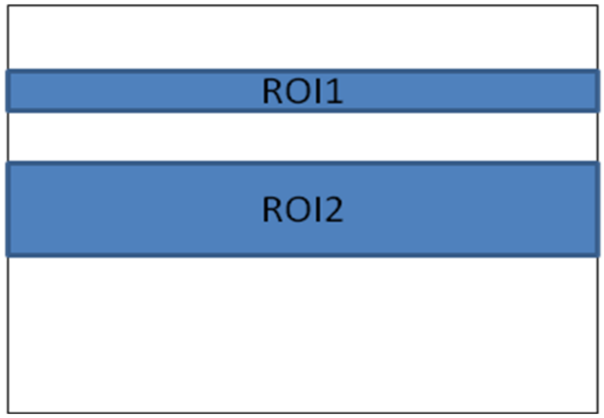

Fig.14. With open access to Row Addressing (11- bit interface to define 1728 rows), AM41 user may construct the image from random lines or groups of lines.

Frame rate goes up approximately as 1/Nrows, where Nrows is the total number of the lines in the selected ROI for one frame. The exact formula for the frame time should include Nrows*One_row_time + Last row read time +VB time. VB time, vertical blank time is the time needed for the Global Transfer operation (TX_n duration), which is normally 1us. If reducing the VB time is critical, the user may overlap the last read time with TX_n time.

If the default sensor clock rate of ~140 MHz is used, yielding 500 Fps at full resolution, then the frame rate can be increased to 1000 frames/s with windowing the sensor down to 864 rows.

If more aggressive clock rate of ~170 Mhz is used, the sensor can reach 1000 Frames per second with 1024-1080 lines. Elevated VDDIO of 2.5V is recommended for higher clock rate.

The sensor is fully functional at 200 Mhz, although the image quality may degrade due to developing of missing codes.

18.0. QUANTUM EFFICIENCY

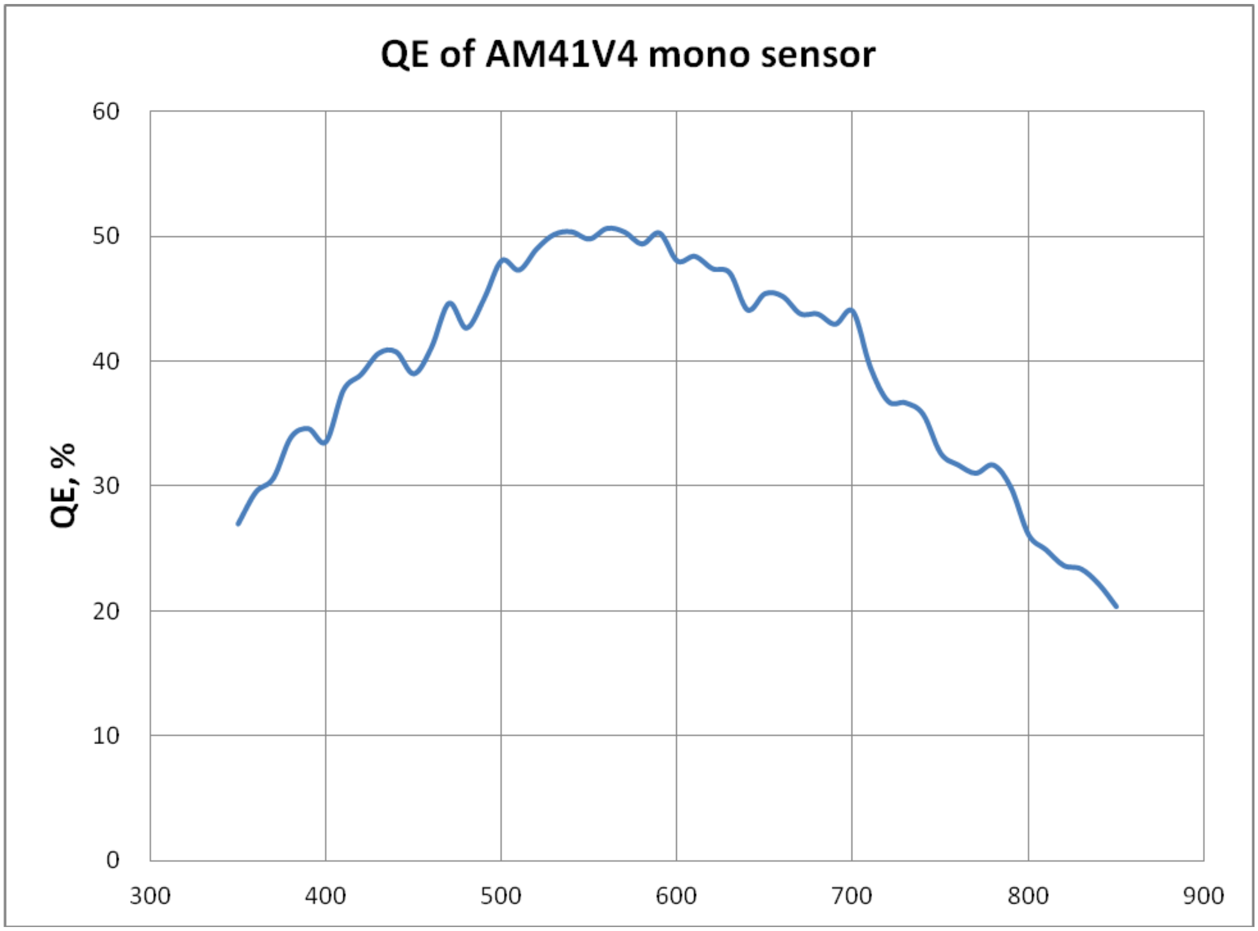

Fig.15. Quantum efficiency of Monochrome AM41V4 sensor

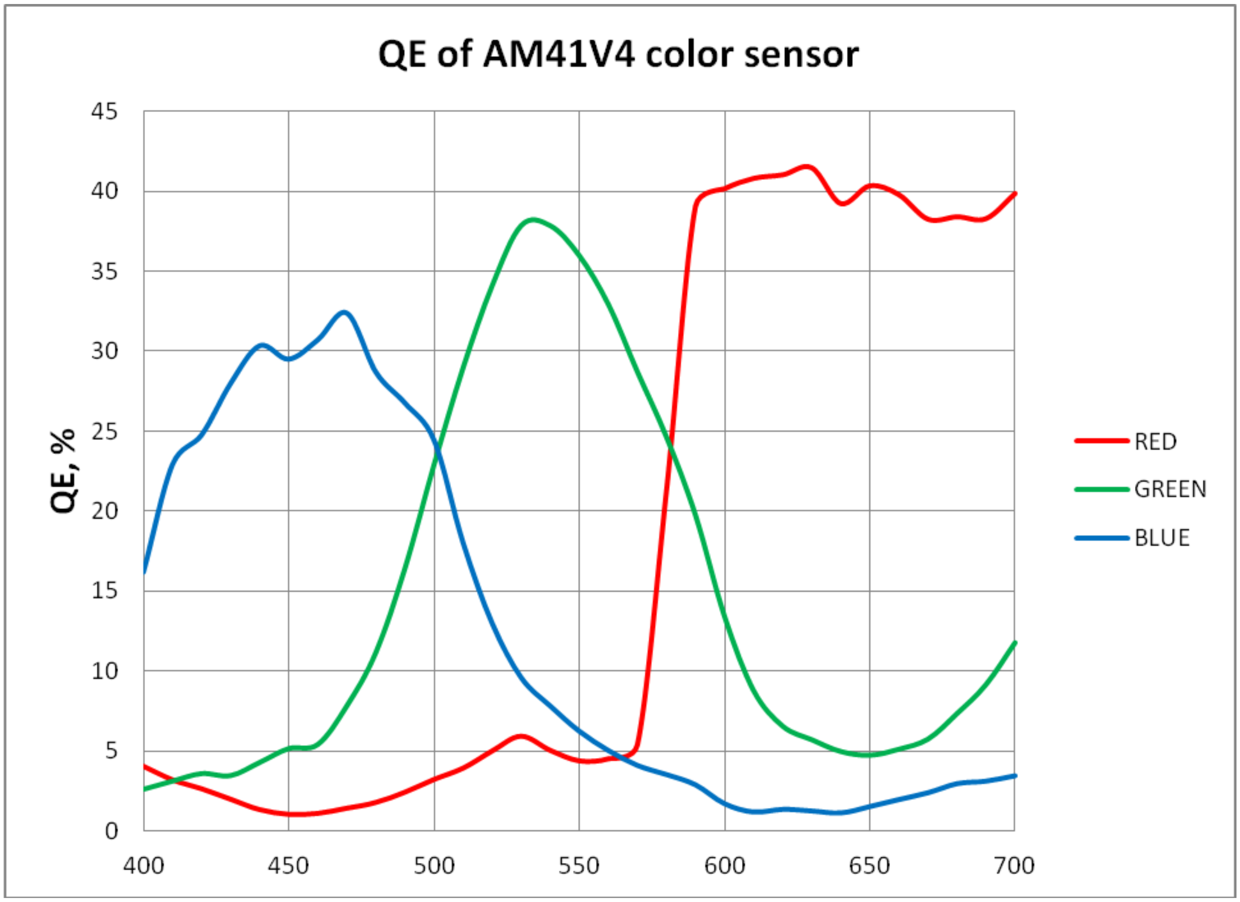

Fig.16. Quantum efficiency of Color AM41V4 sensor

19.0. PACKAGE

- a 1.27mm pitch 280 micro-PGA of ~36mm size.

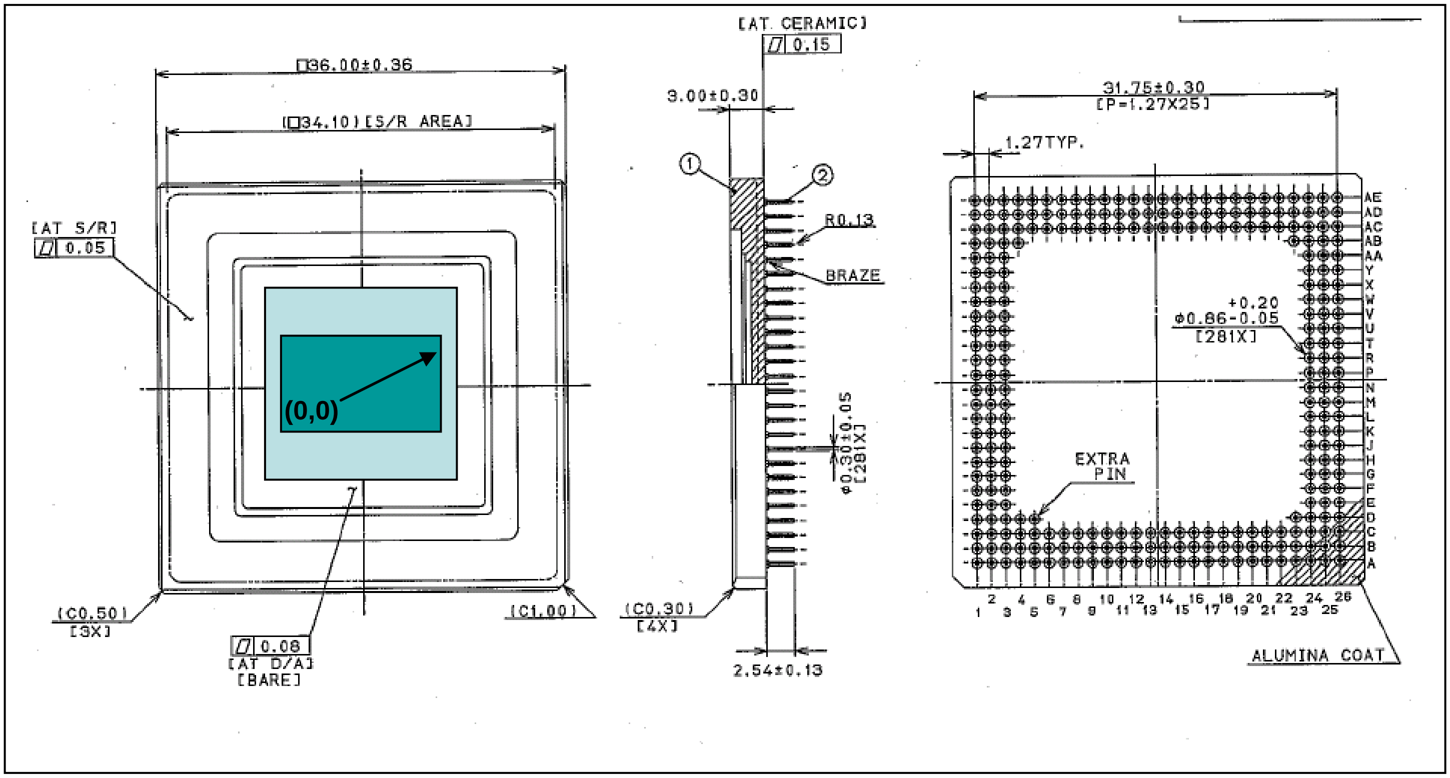

Fig.17. AM41 in 280 micro-PGA package. Chip position and pixel array position in the package is symmetrical top-bottom and left-right.

Not shown on this picture:

Glass thickness 0.8mm
Sensor thickness 0.725mm
Thickness of the package under the cavity: 1.2mm

Regarding the socket for the sensor, try one of the following:
www.andonelect.com 10-26-28-281-414T4-R27-L14
www.onanon.com 1000-281F-0356-01A4 (surface mount)
www.e-tec.com PGA-281-E033-XX-22-MOD-RC (hole through)
www.emilation.com HLS-260281-A-11
Some of these might be custom.